



# **ApolloLake Platforms – Silicon Initialize CodeRVP/CRB BIOS Release Notes**

*Release Notes*

---

*ApolloLake Entry Desktop/Notebook platform based on  
Broxton-P SoC*

*May 2019 (WW18)*

**Intel Confidential**



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

45-nm products are manufactured on a lead-free process. Lead-free per EU RoHS directive July, 2006. Some E.U. RoHS exemptions may apply to other components used in the product package. Residual amounts of halogens are below November, 2007 proposed IPC/JEDEC J-STD-709 standards.

Intel, and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

\*Other names and brands may be claimed as the property of others.

Copyright © 2008, Intel Corporation. All rights reserved.



# Contents

---

Release Note.....	6
1.1 Revision 1.0.0 .....	6
1.2 Revision 1.1.0 .....	6
1.3 Revision 1.1.1 .....	6
Known Issue .....	8
Note .....	9



## ***Table and Figures***

---

**No table of figures entries found.**



## Revision History

---

Document Number	Revision Number	Description	Revision Date
	1.0.0	• Initial Release version	Oct.2017
	1.1.0	• APL MR6 version	Dec.2018
	1.1.1	• APL MR7 version	May.2019



# 1 Release Note

---

## 1.1 Revision 1.0.0

Initial Release

## 1.2 Revision 1.1.0

- Update swizzle calculator spreadsheet. Changed the swizzle value calculation back to fixed offset basis
- Fix HPET UPD in FSP is not work
- InitializeJedec\_DDR3\_Nom60\_Wr0 should be only be called for DramType == TypeDdr3L
- Fix system is unstable and causing stress. idle test fail ,os installation fail and reboot automatically
- Correct UPD description of PortUsb20PerPortRXISet
- Enable the PWM Fan Control in APL FSP MR6
- Fix Intermittent reboot for power management S3 to S0 in Yocto
- APL fails to resume after S3 for >500 cycles
- Locking TCO Base after programming TCO Control register with Base address and enabling it
- Update Support for F1 stepping
- Correct ApolloLake BroxtonSiPkg issue – SmmSmbusProtocol
- Fix QH-MGU\_Start-up problem with negative temperatures – Set Rdcmd2diffampen to 1, Diffampenlenbl4 to 0x3f
- Fix MRC hang at A8 - Save the value of BGF\_RUN (BGF\_RUN\_SAVE) before DunitFreqChangePart1 is executed, and to restore this value after the execution of DunitFreqChangePart3
- Fix ECC boot hangs at MRC checkpoint 30 - Move dllcomp\_reset setting from modmem\_init\_lpddrgrp5p5m\_seq to modmem\_init\_lpddrgrp7\_seq, Toggle dllcomp\_reset from 1->0->1 instead of direct set to 1 - SampleWait\_Max (5->8) - nWR (samsung use nWR to calculate memory frequency)

## 1.3 Revision 1.1.1

- Fix unable to wake up from S3 by Keyboard and Mouse
- Fix PWM Enumeration Cannot Be Found on Yocto
- Reduce SMI latency cause by UEFI GetVariable / SetVariable during OS Run-Time
- Incorporate tuned HCNT, LCNT & Hold values in the BIOS release to meet Hold data rise/fall spec for F1 stepping



## ***Release Note***

- Sensitive Data in MBP Must Not be Exposed to Untrusted Code



## **2      *Known Issue***

---

NA





**Note**

## **3 Note**

---

**Please note the ClientSiliconPkg folder will not update in each milestone release**